



**KPR** Institute of Engineering  
and Technology

(Autonomous)

Avinashi Road, Arasur, Coimbatore - 641 407

**Department of Electronics and Communication Engineering**  
**(Accredited by NBA)**

**NEWSLETTER- DECEMBER 2023 ISSUE**



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## **Vision**

To be a center of excellence for education, research and development in the field of Electronics and Communication engineering to meet the growing needs of the society.

## **Mission**

- Develop competencies in emerging technologies through skill based education collaborating with industries of repute
- Provide conducive environment for research and innovation to cater to the needs of the society
- Inculcate professionalism, ethical values and lifelong learning

## **Programme Educational Objectives**

- PEO1: Apply principles of Electronics and Communication Engineering to provide solutions to the emerging problems in the society.
- PEO2: Embrace technological challenges through skill upgradation or higher education or research.
- PEO3: Exhibit leadership qualities with professional and ethical values

## EVENT ORGANIZED

- The department of ECE has organised the Industry one Credit Course on Robotics Operating System for third year students. Dr M.Kalamani and Dr R.Jaikumar conducted this course during 08.12.2023 to 09.12.2023. Resource person Mr.Karthik Sundar, Technical Lead – Sensors and Algorithms, MulticoreWare India Private Limited, Coimbatore handled the hands on session and 22 students benefited from his session.

The poster is for a one-credit course titled "ROBOTIC OPERATING SYSTEM" organized by the Department of ECE at KPR Institute of Engineering and Technology. The course is led by Mr. Karthik Sundar, Tech lead Sensors and Algorithm Sensor TU Multicoreware. The course dates are 08.12.2023 & 09.12.2023, from 9.00AM to 5.00PM, for III YEAR ECE - B students. The poster also includes the KPR Institute of Engineering and Technology logo, the Department of ECE logo, and a portrait of Mr. Karthik Sundar. The website kpriet.edu.in and social media icons are also present.

- Mr.Nepolean Mani, Senior Design Engineer, Bangalore, addressed the participants. This Industrial training focused on VLSI Design Flow, Revised Digital Concepts, Verilog and System Verilog Programming and RTL design and verification concepts. The session was lively with active students interaction. Students learnt Digital Design and Verification concepts for entire training session.



Most of the students were satisfied with the various aspects of teaching like coverage of syllabus in class, emphasis on fundamentals, coverage of modern/advanced topics and overall program with live practical examples in open source tool. 93% students felt that the VLSI programme is easy and 90% students felt that the instructions were easy to follow. 92.7% students responded that reading materials and reference books regarding subjects were easily found. 96% students commented that the training was relevant to job and future aspirations thus indicating that this training provides larger scope for employability. 96% students felt that the course helped them in building their job aspire.



- The two-day workshop on VLSI Design Flow using Cadence Tools aimed to provide participants with in-depth knowledge and hands-on experience in the field of Very Large Scale Integration (VLSI) design. The workshop focused on utilizing Cadence tools throughout the design flow, covering key stages such as specification, design, verification, synthesis and layout. The workshop agenda included the following key sessions on Introduction to Semi-Custom IC Design Flow, Functional Verification using Incisive, RTL Synthesis using Genus Synthesis Solution, Physical Implementation using Innovus that includes Floor Planning, Power Planning, Placement, CTS, Routing, Verification checks like DRC, connectivity, Parasitic Extraction, Generation of GDSII, Introduction to Full Custom IC Design Flow, Capture using Virtuoso Schematic Editor, Symbol Creation, Testbench Creation using Virtuoso Symbol Editor, Functional Simulation using Spectre, Layout Design using Virtuoso Layout Suite, Physical Verification which includes DRC & LVS, Parasitic Extraction using Quantus, Post Layout

Simulation, Generation of GDSII. The workshop began with an insightful introduction to VLSI design and an overview of the Cadence tool suite. The resource person is an industry expert Mr. Priyanshu Datta, Entuple Technologies with extensive experience, provided valuable insights into the latest trends and best practices in the field. Participants actively engaged in hands-on sessions using Cadence tools for schematic entry, simulation, synthesis, and layout. The workshop included showcasing successful applications of VLSI design using Cadence tools. The Workshop on VLSI Design Flow using Cadence Tools proved to be a valuable learning experience for participants, providing them with practical skills, industry insights, and a deeper understanding of the VLSI design process. The event successfully fostered collaboration and networking within the VLSI community.

**KPR Institute of Engineering and Technology**  
Learn Beyond (Autonomous, NAAC "A")

**TWO DAYS WORKSHOP ON VLSI DESIGN FLOW USING CADENCE TOOL**

22.12.2023 & 23.12.2023  
9.00 AM to 4.00 PM  
Digital Systems and Networks Lab

**DEPARTMENT OF ECE**

**Mr. Priyanshu Datta**  
Field Application Engineer (FAE) in Entuple Technologies

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INSTITUTE OF TECHNICAL EDUCATION

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## FACULTY PUBLICATIONS

- **Jagadesh Sambantham**, Gomathy Balasubramanian, Rajarathnam, & Mohit Tiwari. (2023). A linear differentiation scheme for camouflaged target detection using convolution neural networks. RAiSE-2023. <https://doi.org/10.3390/engproc2023059045>
- A Arul, **M Kathirvelu**. (2023). Design of a novel 1-bit full adder with hybrid logic for full-swing, area-efficiency, and high-speed. Integration, 102123. <https://doi.org/10.1016/j.vlsi.2023.102123>

- Vijaya, K. S., Chandana, B. H. ., Sugumar, D., **J.Muralidharan**. Moahana Krishna, I. Ramesh babu P (2023). Automated Seizure Detection Using Machine Learning Algorithm in Very Large Scale Integration. International Journal of Intelligent Systems and Applications in Engineering, 12(7s), 01–06. Retrieved from <https://ijisae.org/index.php/IJISAE/article/view/4002>

### FACULTY PARTICIPATION

Name of the Faculty	Title of FDP/STTP/OFDP/Conference/Online Course	Organization Name	Start Date	End Date
Dr.S.M.Ramesh	Low power adders for efficient image processing applications	Vidya Vihar Institute of Technology, Bihar & KCT Tech Park, Coimbatore	12/22/2023	12/22/2023
Dr.S.M.Ramesh	An In-Depth Exploration Of Autism Spectrum Disorders Through Machine Learning Analysis	Lincoln University, Malaysia & Dr.NGPIT, Coimbatore	12/2/2023	12/2/2023
Dr.M.Kalamani	Web-Based System for Detecting Plant Leaf Diseases and Providing Treatment Recommendation	MIR Labs	12/14/2023	12/14/2023
Dr.N.SathishKumar	Antenna Design using CST	Vellore Institute of Technology	12/4/2023	12/8/2023
Mr.G.Pradeepkumar	Research Opportunities in Medical Image Processing	Chaitanya Bharathi Institute of Technology	11/27/2023	12/2/2023
Dr.J.Muralidharan	Unveiling New Avenues in the Design of Next Generation Semiconductor Devices	KGISL INSTITUTE OF TECHNOLOGY	12/18/2023	12/23/2023

### PLACEMENT ACTIVITIES

S.No	Name of the Student	Name of the Company	Package
1	Kavin Raj S	Lavendel Consulting	6.5LPA

2	Aswin MM	Lavendel Consulting	6.5LPA
3	Mohanraj M	Lavendel Consulting	6.5LPA
4	Navaneethakrishnan G	Lavendel Consulting	6.5LPA
5	Dharun Karthik R	Lavendel Consulting	6.5LPA
6	Deepak R	Teachnook	4LPA
7	Kavin P	Teachnook	4LPA
8	Sachin A M	Teachnook	4LPA

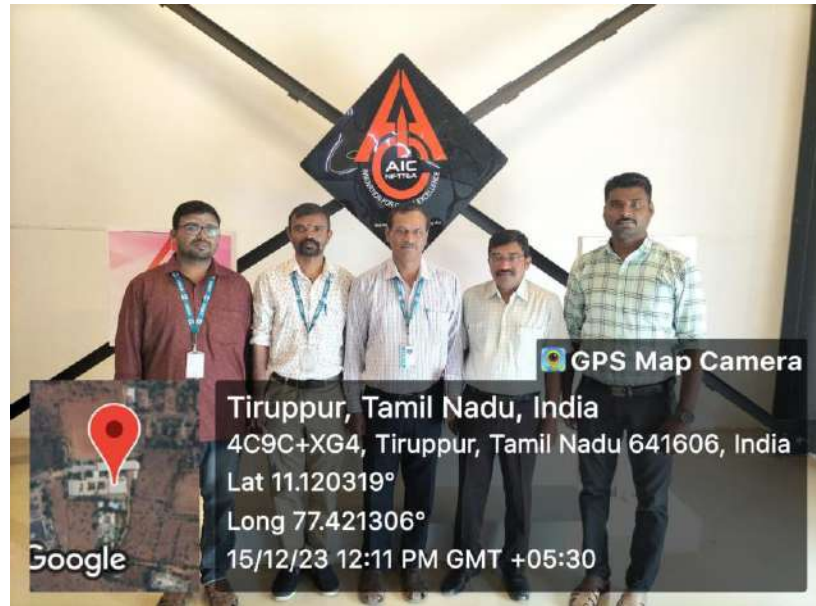
## IIPC ACTIVITIES

### INDUSTRY VISITS



- Dr.K.S.Tamilselvan, Mr.S.Balamurali and Mr.S.Satheeshkumar visited M/s.NIFT-TEA, Tiruppur on 15.12.2023 and discussed about student internship and collaborative research projects.
- Mr.S.Balamurali, Mr.S.Satheeshkumar and Dr.K.S.Tamilselvan visited M/s.Global Tex Machines, Tiruppur on 15.12.2023 and discussed about consultancy works in industrial automation.





- Mr.S.Satheeshkumar, Mr.S.Balamurali, and Dr.K.S.Tamilselvan visited M/s.Swathi Hatcheries, Palladam on 15.12.2023 and discussed about consultancy works in Hatchery automation and Poultry farms.



## OTHER ACTIVITIES

Organized a one-week industrial training program on “Design and verification concepts using EDA tools” in association with Tessolve Semiconductor Pvt. Ltd., Bangalore from 12.12.2023 to 16.12.2023. Totally, 43 students from the III-year ECE participated and got benefited.

